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(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Bruce W. MCGAUGHY et al.

Application No.: 10/713,729 | Confirmation No.: 2684

Filed: November 13, 2003 | Art Unit: 2128

For: SYSTEM AND METHOD FOR DYNAMICALLY COMPRESSING CIRCUIT COMPONENTS DURING SIMULATION | Examiner: D. Silver

**RESPONSE TO NON-COMPLIANT APPEAL BRIEF (37 CFR 41.37)**

MS AF
Commissioner for Patents
P.O. Box 1450
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Dear Sir:

## INTRODUCTORY COMMENTS

This is in response to the final Office Action dated October 15, 2007 (Paper No. 20071012), for which a response was due on November 15, 2007. Accordingly, this response is timely filed. Reconsideration and allowance of the pending claims, as amended, in light of the remarks presented herein are respectfully requested.

**Summary of Claimed Subject Matter** is resubmitted per communication dated 10/15/2007, which begins on page 2 of this paper.

## SUMMARY OF CLAIMED SUBJECT MATTER

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed inventions are directed to a system and method for dynamically compressing circuit components represented in a hierarchical data structure during simulation. According to an embodiment of the present invention, a method of simulating a circuit having a hierarchical data structure comprises selecting a group of leaf circuits from a first branch and a second branch of the hierarchical data structure for simulation, representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior, creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit, where the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits, simulating the group of leaf circuits in accordance with the first port connectivity interface, and storing simulation results of the group of leaf circuits in a memory device.

In addition, per paragraphs 4 and 10 of the communication dated 10/15/2007, Applicants have mapped the independent claims 1, 9, and 17 to the corresponding drawings and specifications according to embodiments of the present invention. Specifically, the independent claims 1, 9, 17 are at least supported by Figure 7, Figure 12B, Figures 14A-14C, and their corresponding descriptions in paragraphs [0025]-[0026] (pages 19-20), [0049]-[0050] (pages 32-33), and [0059]-[0063] respectively. For the convenience of the Board and the Examiner, numerals from the Figures illustrating the corresponding claim elements are added in claims 1, 9, and 17 below in parenthesis.

Note that a minor amendment is made to claims 1, 9, and 17 to correct an antecedent basis error which was inadvertently introduced in the January 25, 2007 Amendment in Response to Non-Final Office Action. The original claims did not have this antecedent basis error. No new matters have been added.

Claim 1 (Currently amended): A method of simulating a circuit having a hierarchical data structure, comprising:

representing the circuit as a hierarchically arranged set of branches (**Figure 14B**), including a root branch (**1400**) and a plurality of other branches (**1420, 1440**) logically organized in a graph; the hierarchically arranged set of branches (**Figure 14B**) including a first branch (**1420**) that includes one or more leaf circuits (**1425**) and a second branch (**1440**) that includes one or more leaf circuits (**leaf circuits referenced by 1417**); wherein the first branch (**1420**) and second branch (**1440**) are interconnected in the graph through a third branch (**1400**) at a higher hierarchical level in the graph than the first and second branches (**1420, 1440**);

selecting a group of leaf circuits (**1425, leaf circuits referenced by 1417**), from the first and second branches (**1420, 1440**) for simulation;

representing [[the]] two or more leaf circuits as a merged leaf circuit (**1418**) in response to the two or more leaf circuits of the circuit having a substantially same isomorphic behavior;

creating a first port connectivity interface (**1432, 1220**) dynamically for the group of leaf circuits in response to the merged leaf circuit (**1418**); wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

simulating the group of leaf circuits (**1425, 1417, 1418**) in accordance with the first port connectivity interface (**1432, 1220**).

Claim 9 (Currently amended): A system for simulating a circuit having a hierarchical data structure, comprising:

at least one processing unit (**700**) for executing computer programs;

a user interface (**702**) for performing at least one of the functions selected from the group consisting of entering a netlist representation of the circuit, viewing representations of the circuit on a display, and observing simulation results of the circuit;

a memory (**704**) for storing static and dynamic information of the circuit;

a simulator module (**712**) for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit, a user interface and a memory, and the simulator module includes:

means for representing the circuit (**700, 702, 708, 712**) as a hierarchically arranged set of branches (**Figure 14B**), including a root branch (**1400**) and a plurality of other branches (**1420, 1440**) logically organized in a graph; the hierarchically arranged set of branches (**Figure 14B**) including a first branch (**1420**) that includes one or more leaf circuits (**1425**) and a second branch (**1440**) that includes one or more leaf circuits (**leaf circuits referenced by 1417**); wherein the first branch (**1420**) and second branch (**1440**) are interconnected in the graph through a third branch (**1400**) at a higher hierarchical level in the graph than the first and second branches (**1420, 1440**);

means for selecting a group of leaf circuits (**700, 702, 708, 712, 1425, leaf circuits referenced by 1417**), from the first and second branches (**1420, 1440**) for simulation;

means for representing [[the]] two or more leaf circuits (**700, 702, 708, 712**) as a merged leaf circuit (**1418**) in response to the two or more leaf circuits of the circuit having a substantially same isomorphic behavior;

means for creating a first port connectivity interface ((**700, 702, 708, 712, 1432, 1220**) dynamically for the group of leaf circuits in response to the merged leaf circuit (**1418**); wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

means for simulating the group of leaf circuits (**700, 702, 708, 712, 1425, 1417, 1418**) in accordance with the first port connectivity interface (**1432, 1220**).

Claim 17 (Currently amended): A computer program product, comprising a medium storing computer programs for executing by one or more computer systems, the computer program comprising:

a simulator module (**712**) for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit (700) , a user interface (**702**) and a memory (**704**), and the simulator module includes one or more computer programs containing instructions for:

representing the circuit as a hierarchically arranged set of branches (**Figure 14B**), including a root branch (**1400**) and a plurality of other branches (**1420, 1440**) logically organized in a graph; the hierarchically arranged set of branches (**Figure 14B**) including a first branch (**1420**) that includes one or more leaf circuits (**1425**) and a second branch (**1440**) that includes one or more

leaf circuits (**leaf circuits referenced by 1417**); wherein the first branch (**1420**) and second branch (**1440**) are interconnected in the graph through a third branch (**1400**) at a higher hierarchical level in the graph than the first and second branches (**1420, 1440**);

selecting a group of leaf circuits (**1425, leaf circuits referenced by 1417**), from the first and second branches (**1420, 1440**) for simulation;

representing [[the]] two or more leaf circuits as a merged leaf circuit (**1418**) in response to the two or more leaf circuits of the circuit having a substantially same isomorphic behavior;

creating a first port connectivity interface (**1432, 1220**) dynamically for the group of leaf circuits in response to the merged leaf circuit (**1418**); wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits; and

simulating the group of leaf circuits (**1425, 1417, 1418**) in accordance with the first port connectivity interface (**1432, 1220**).

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Respectfully submitted,

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